SPECIFICATION AMENDMENTS

Please replace the paragraph beginning on page 1, line 3 with the following amended paragraph:

A1 ~~The~~ This invention generally relates to power reduction in a memory bus interface.

Please replace the paragraph beginning on page 3, line 3 with the following amended paragraph:

A2 Fig. 11 is a schematic diagram of ~~control circuitry for~~ read buffer circuitry and control circuitry coupled to a sense amplifier according to an embodiment of the invention.

Please replace the paragraph beginning on page 3, line 11 with the following amended paragraph:

A3 Referring to Fig. 1, an embodiment ~~10~~ of a computer system 10 in accordance with the invention includes a system memory 22 for storing various data associated with the operation of the computer system 10. The system memory 22 is formed from a collection of semiconductor memory devices. As an example, the system memory 22 may include double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices.

Please replace the paragraph beginning on page 6, line 16 with the following amended paragraph:

A4 Referring to Fig. 2, in some embodiments of the invention, the memory controller hub 16 may include the memory controller 18 to communicate with the memory bus 20; a system bus interface 70 to communicate with a system bus 14 of the computer system 10; an Accelerated Graphics Port (AGP) bus interface 74 to communicate with an AGP bus 26 (Fig. 1) of the computer system; and a hub interface 72 to communicate with a south bridge, or input/output (I/O) ~~I/O~~ hub 40, of the computer system over hub link 34. The AGP is described in detail in the Accelerated Graphics Port Interface Specification, Revision 1.0, published on July 31, 1996, by Intel Corporation of Santa Clara, California. The memory controller 18, system bus interface 70,

A4 AGP bus interface 74 and hub interface 72 are all coupled together to communicate data to various parts of the computer system 10.

Please replace the paragraph beginning on page 7, line 7, with the following amended paragraph:

The data interface 100 also includes ~~a~~ circuitry associated with the read path of the data interface 100. In this manner, the data interface 100 includes sense amplifiers 102 that are A5 coupled to receive data bit line signals (called DQ[0:63], which represents sixty-four DQ data bit lines as an example) from respective data bit lines 104 of the memory bus 20. The enablement/disablement of the sense amplifiers 102 is controlled by a sense amplifier control circuit 114. In this manner, as further described below, in response to the beginning of a read operation, the sense amplifier control circuit 114 enables the sense amplifiers 102, and in response to the end of a particular read operation (and no subsequent read operation), the sense amplifier control circuit 114 disables the sense amplifiers 102.

Please replace the paragraph beginning on page 7, line 23 with the following amended paragraph:

Among the other circuitry of the data interface 100, the data interface 100, in some embodiments of the invention, includes a delay circuit 108 that is coupled to the DQS data strobe line 106 to receive the DQS data strobe signal. The delay circuit 108 delays the DQS data strobe A6 signal to produce a delayed data strobe signal (such as the signal depicted in Fig. 8) that appears on a clock signal line 103 that clocks operations of a <u>read</u> data buffer 112, as further described below. In some embodiments of the invention, the delay circuit 108 delays the DQS data strobe by one quarter period of a system clock signal (called SCLK). The SCLK system clock signal, in turn, may be used, for example, on the output side of the read data buffer 112 to read the sample data from the read data buffer 112. Furthermore, the frequency of the SCLK signal may be approximately the same as the frequency of the DQS strobe signal when driven.

Please replace the paragraph beginning on page 8, line 22 with the following amended paragraph:

A7 ~~As depicted in Fig. 9, the~~ The flip-flop 154 receives the EOB signal, depicted in Fig. 9, at its input signal terminal, and the clock terminal of the flip-flop 154 is connected to the output terminal of an inverter 152 that receives the internal read ~~delay~~ delayed DQS data strobe signal, i.e., the input terminal of the inverter 152 is coupled to the communication line 103. The flip-flop 154 is clocked on the positive going edges of the clock signal present at its clock terminal. Therefore, the flip-flop 154 is clocked on the negative going edges of the delayed DQS signal. The non-inverted output terminal of the flip-flop 154 is coupled to one input terminal of an AND gate 107, and the output terminal of the AND gate 107 furnishes the EN# signal.

Please replace the paragraph beginning on page 8, line 30 with the following amended paragraph:

A8 The memory controller 18 uses the circuitry 200 in the following manner. In a particular read operation (a burst read operation, for example) before the last negative going edge of the DQS data strobe signal, the control circuit 142 (Fig. 3) asserts (drives high, for example) the EOB signal. For the example depicted in Fig 9, the control circuit 142 asserts the EOB signal around time T_5. The flip-flop 154 responds to the negative going edge of the delayed DQS data strobe signal by driving high the voltage of its non-inverted output terminal. This causes the AND gate 107 to deassert (drive high, for example) the EN# signal. For the example depicted in Fig. 10, this deassertion of the EN# signal occurs at time T_6. Therefore, in response to the last negative going edge of the delayed DQS data strobe signal, the flip-flop 154 disables the sense amplifier 102.

Please replace the paragraph beginning on page 9, line 20 with the following amended paragraph:

A9 The circuitry 200 depicted in Fig. 11 also includes latches 150 and 151, circuitry of the read data buffer 112. In this manner, the read data buffer 112 includes the latches 150 and 151 for each data bit line of the memory bus 20. The latch 150 captures its input from the output

terminal of the sense amplifier 102 in synchronization with the negative going edge of the delayed DQS data strobe signal, and thus, its latching trigger input terminal is coupled to the

A9 ~~input terminal 103 of the buffer~~ output terminal 103 of the inverter 152. The latch 151 captures its input from the output terminal of the sense amplifier 102 in synchronization with the positive going edge of the delayed DQS data strobe signal, and thus, its latching trigger input terminal is coupled to the input terminal 103 of the ~~buffer~~ inverter 152. The non-inverting output terminals of the latches provide signals indicative of captured bits of data to respective communication lines 113.

Please replace the paragraph beginning on page 9, line 30 with the following amended paragraph:

A10

Other embodiments are within the scope of the following claims. For example, the circuitry of the memory controller 18 may be used in a similar fashion in a particular memory device of the system memory 22. In this manner, referring to Fig. 12, in some embodiments of the invention, a particular system memory device 220 may include, for example, the data interface 100 described above in connection with the memory controller 18. Thus, for these embodiments, instead of disabling the sense amplifiers of the memory device in response to the absence of a read operation, the interface 100 disables the memory device 220 in the absence of a write operation, i.e., an operation in which data is received from the memory controller 18. Other variations are within the scope of the following claims.

Please replace the paragraph beginning on page 10, line 15 with the following amended paragraph:

A11

The memory controller hub 16 may communicate over the hub link 34 to the I/O hub 40 that, in turn provides an interface to an I/O expansion bus 42 and a Peripheral Component Interconnect (PCI) bus 60. The PCI Specification is available from The PCI Special Interest Group, Portland, Oregon 97214. An I/O controller 44 may be coupled to the I/O expansion bus 42 and may receive input from a mouse 46 and a keyboard 48. The I/O controller 44 may also control operations of a floppy disk drive 50. The I/O hub 40 may control operations of a ~~CD-~~

A11 ~~ROM~~ compact disk read-only memory (CD-ROM) drive 52 as well as control operations of a hard disk drive 54. The PCI bus 60 may be coupled to a network interface card (NIC) that is connected to a network to establish communications between the computer system 10 and the network. Other variations of the computer system 10 are possible.

Please replace the paragraph beginning on page 10, line 25 with the following amended paragraph:

A12 While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of ~~this~~ the present invention.

Please replace the Abstract with the following:

Sub B1

A13 ~~A technique includes amplifying data signals from a memory bus interface. The amplified data signals are sampled, and the amplifier is selectively disabled in response to the absence of a predetermined operation occurring over the memory bus.~~ A method and apparatus for selectively disabling sense amplifiers to reduce power consumption in a [computer system] memory bus interface are disclosed. The method includes amplifying data signals from a memory bus interface. The amplified data signals are sampled, and the amplifier is selectively disabled in response to the absence or end of a predetermined operation occurring over the memory bus. In some embodiments of the invention, the amplification may be selectively enabled in response to the beginning of the predetermined operation over the memory bus. According to some embodiments, the disabling of the amplification may be synchronized to an edge of a delayed data strobe signal. In some embodiments, signals associated with a double data rate ("DDR") synchronous dynamic random access memory ("SDRAM") device may be communicated over the memory bus.